

FIG. 1A
(PRIOR ART)

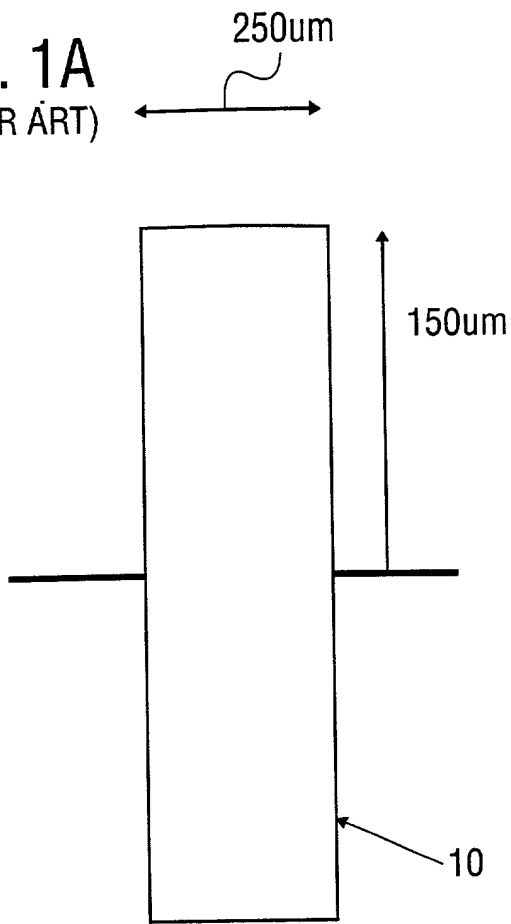


FIG. 1B
(PRIOR ART)

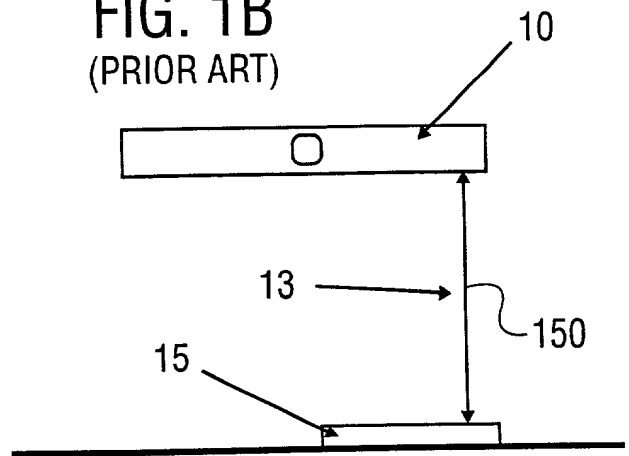


FIG. 1C
(PRIOR ART)

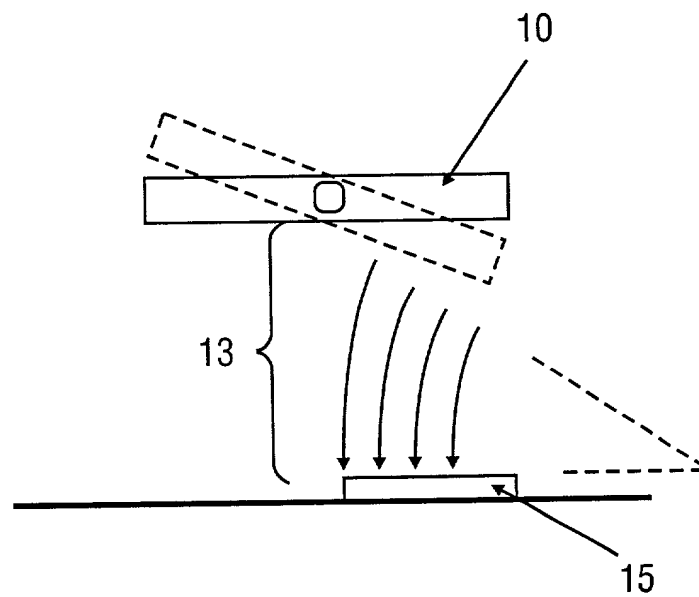


FIG. 3A

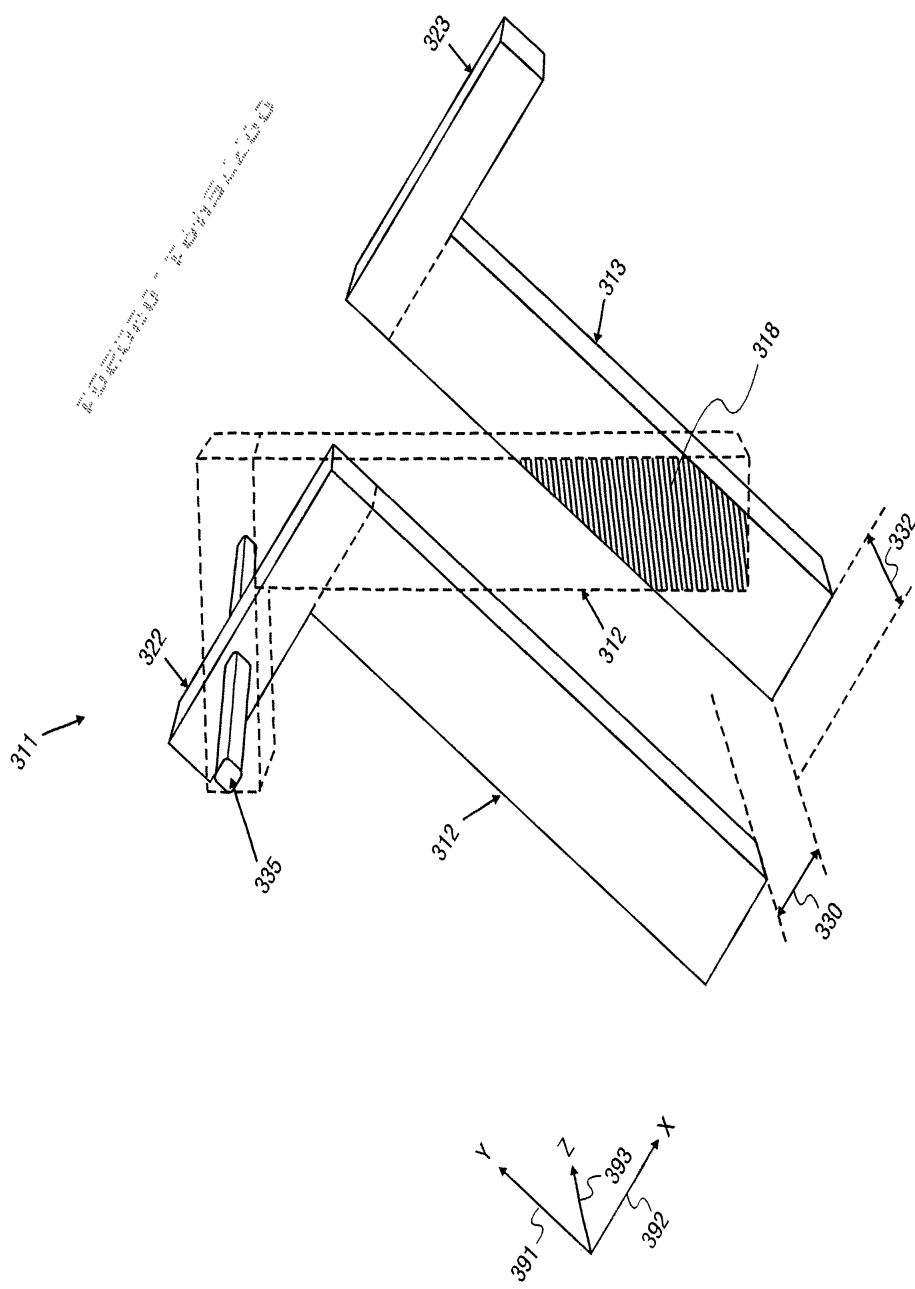


FIG. 3B

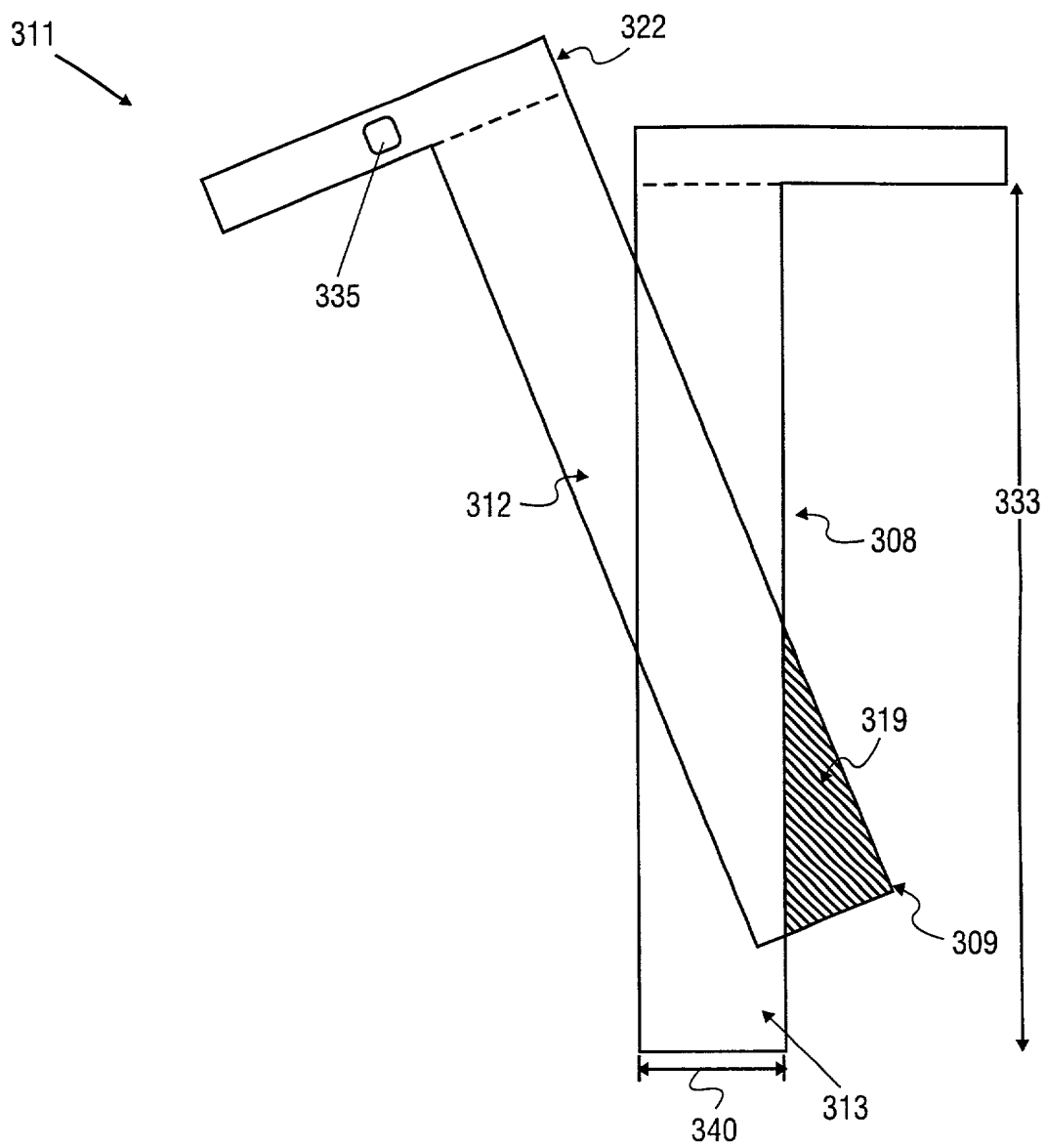


FIG. 3C

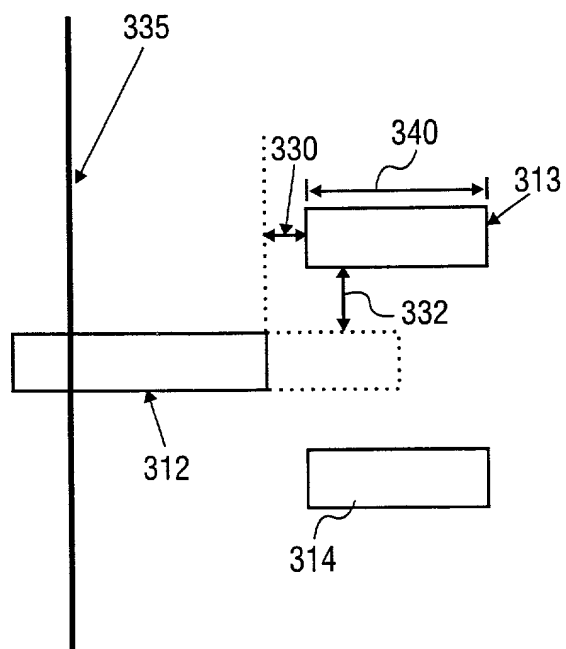
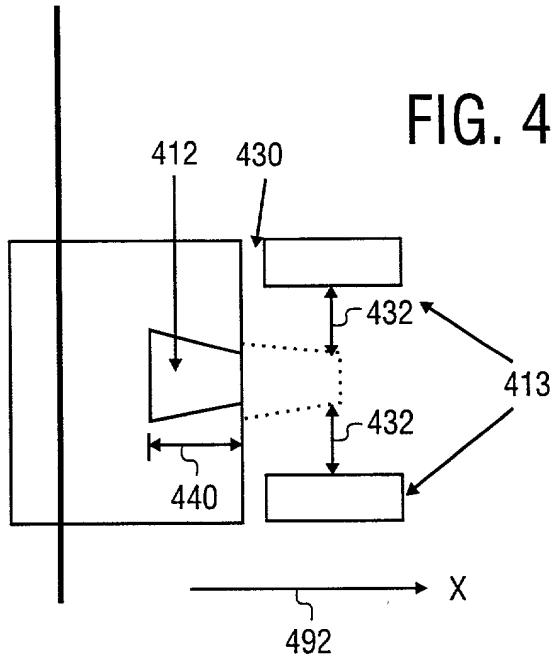


FIG. 3D

FIG. 4 is a schematic diagram of a device 400 in a cross-sectional view. The device 400 includes a substrate 410, a gate stack 412, a gate electrode 413, a channel layer 414, a source/drain region 415, and a contact layer 416. The gate stack 412 is formed on the substrate 410 and includes a gate oxide layer 412a and a gate electrode layer 412b. The gate electrode 413 is formed on the gate stack 412 and is electrically connected to the gate oxide layer 412a. The channel layer 414 is formed on the gate electrode 413 and is electrically connected to the gate electrode layer 412b. The source/drain region 415 is formed on the channel layer 414 and is electrically connected to the channel layer 414. The contact layer 416 is formed on the source/drain region 415 and is electrically connected to the source/drain region 415. The device 400 is shown in a cross-sectional view along a line X-X'.



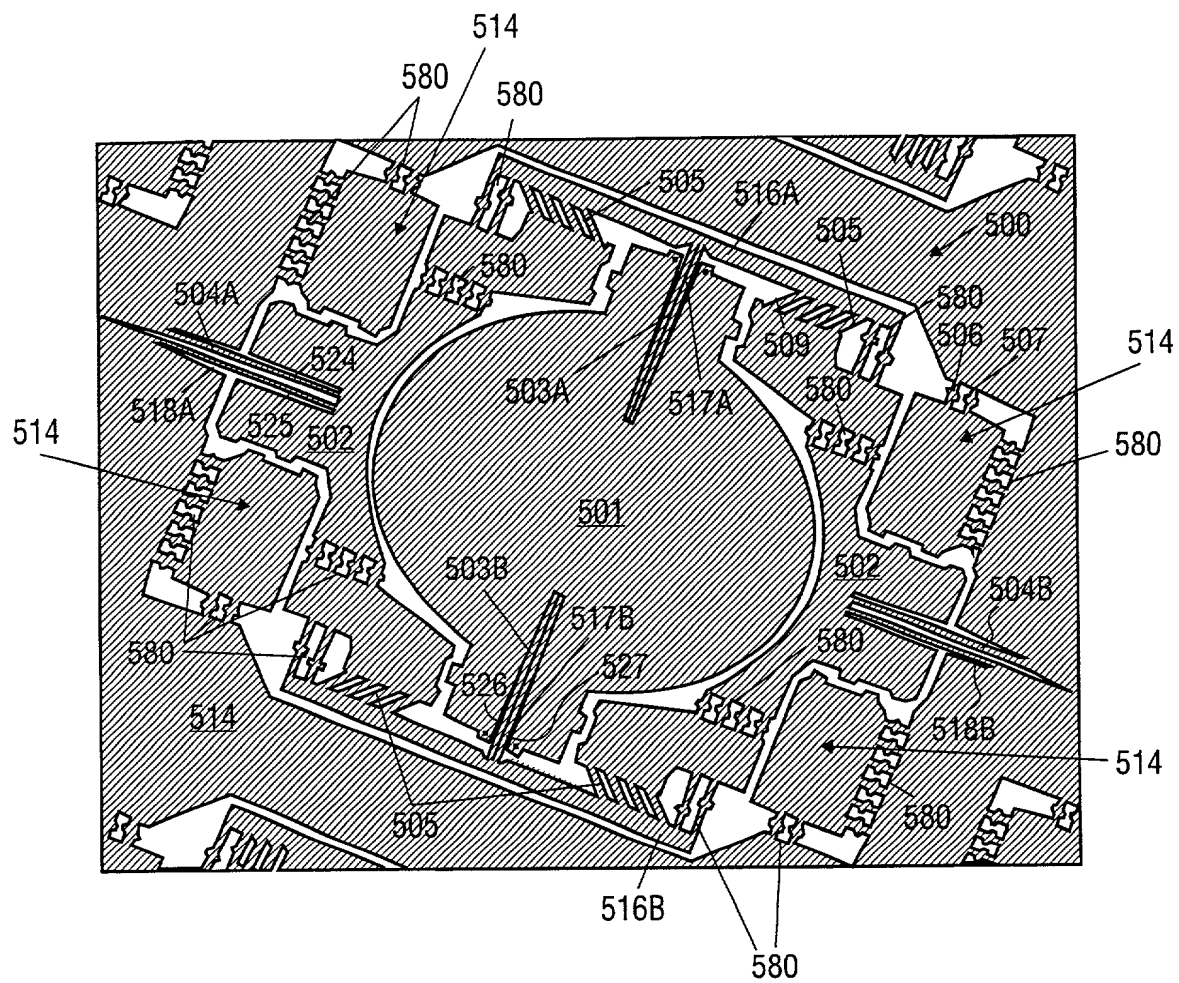


FIG. 5A

FIG. 5B is a cross-sectional view of the device 500 taken along line 500A of FIG. 5A, showing the device 500 in a first position. The device 500 includes a base 501, a central shaft 502, and a plurality of blades 503. The blades 503 are arranged in a row and are connected to the central shaft 502 by a plurality of hinges 504. The blades 503 are shown in a first position, which is a closed position. The device 500 is shown in a first position, which is a closed position.

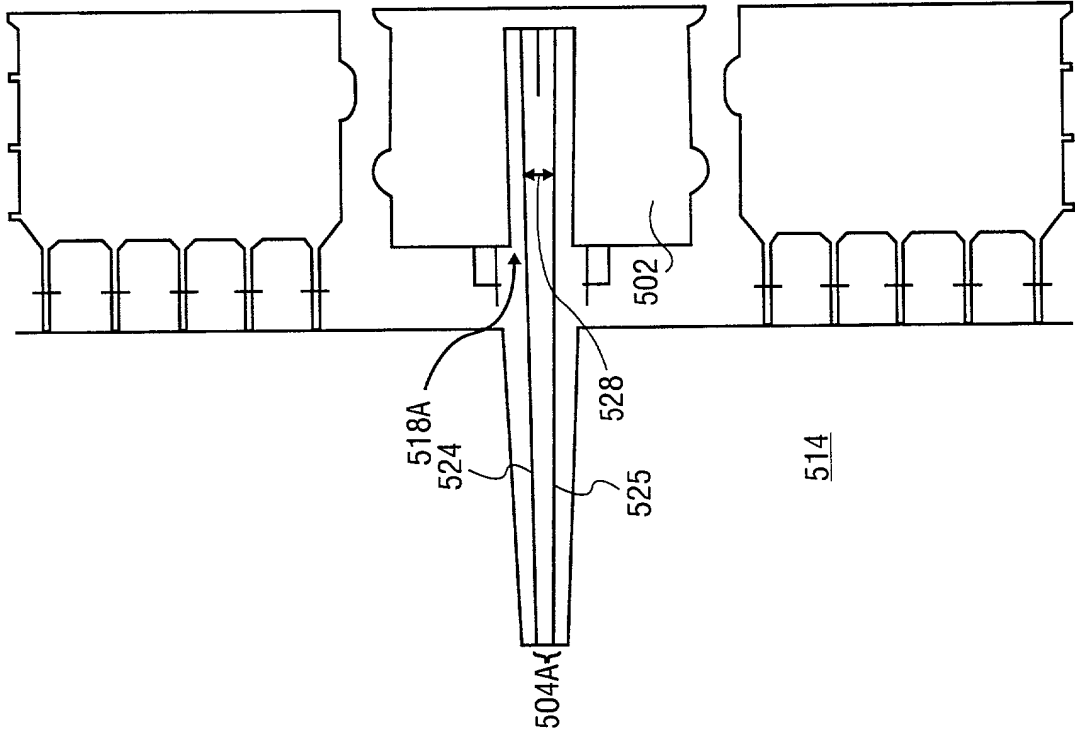


FIG. 5B

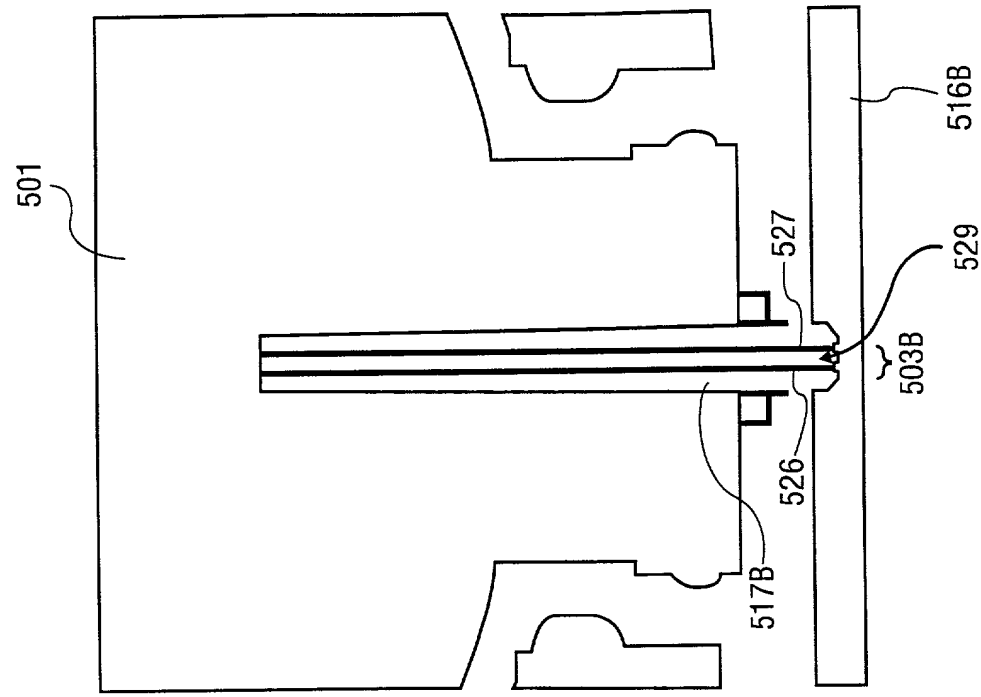


FIG. 5C

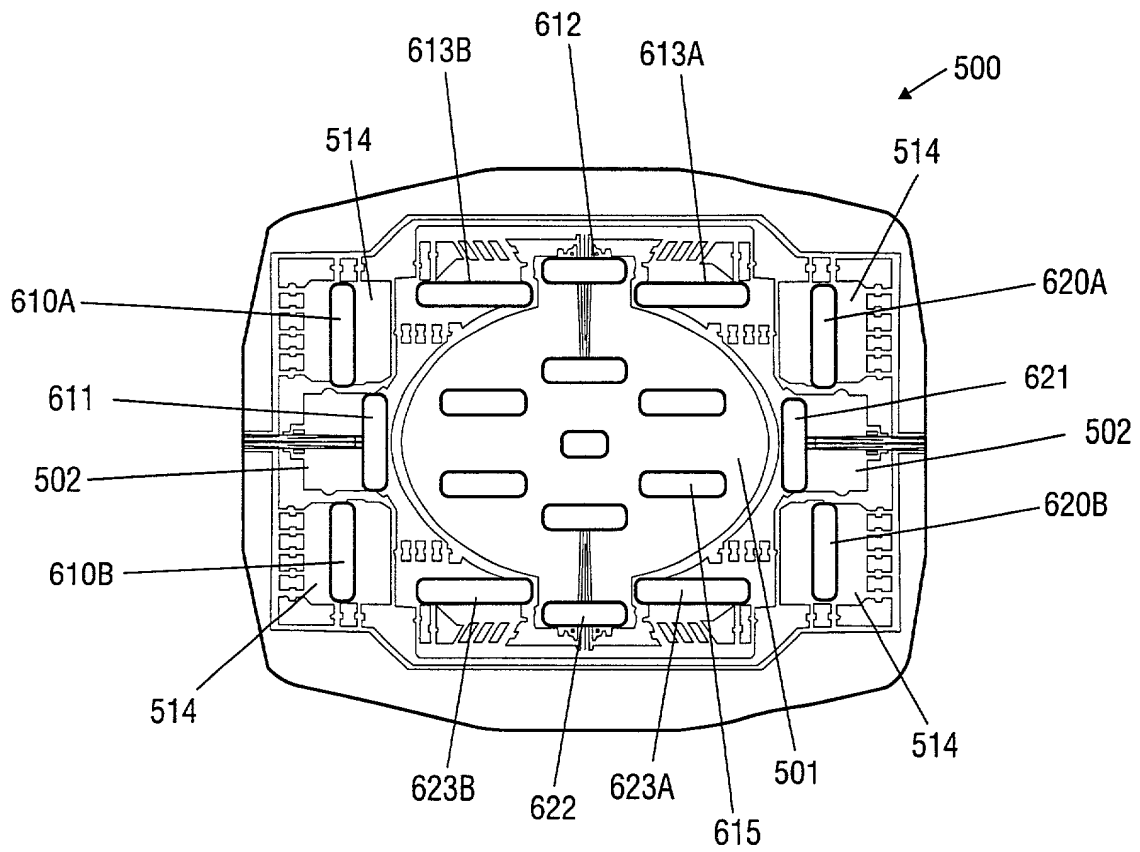


FIG. 6

FIG. 7A is a top view of a semiconductor device 700. The device 700 includes a substrate 701, a gate stack 702, a source/drain region 703, a gate electrode 704, a gate spacer 705, a gate contact 706, a gate pad 707, a gate line 708, a gate bus 709, a gate pad 710, a gate contact 711, a gate spacer 712, a gate electrode 713, a source/drain region 714, a gate stack 715, and a substrate 716.

700

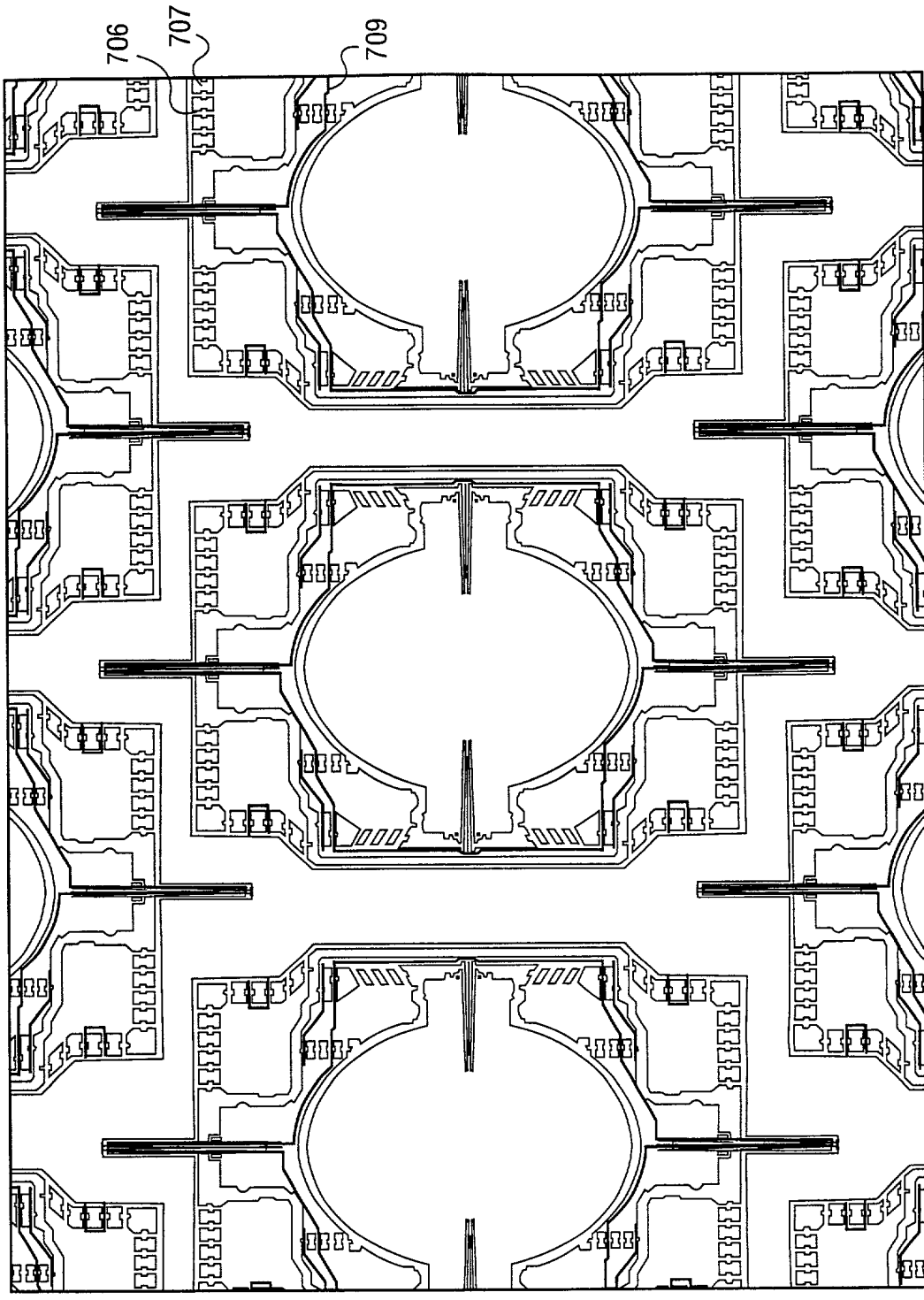


FIG. 7A

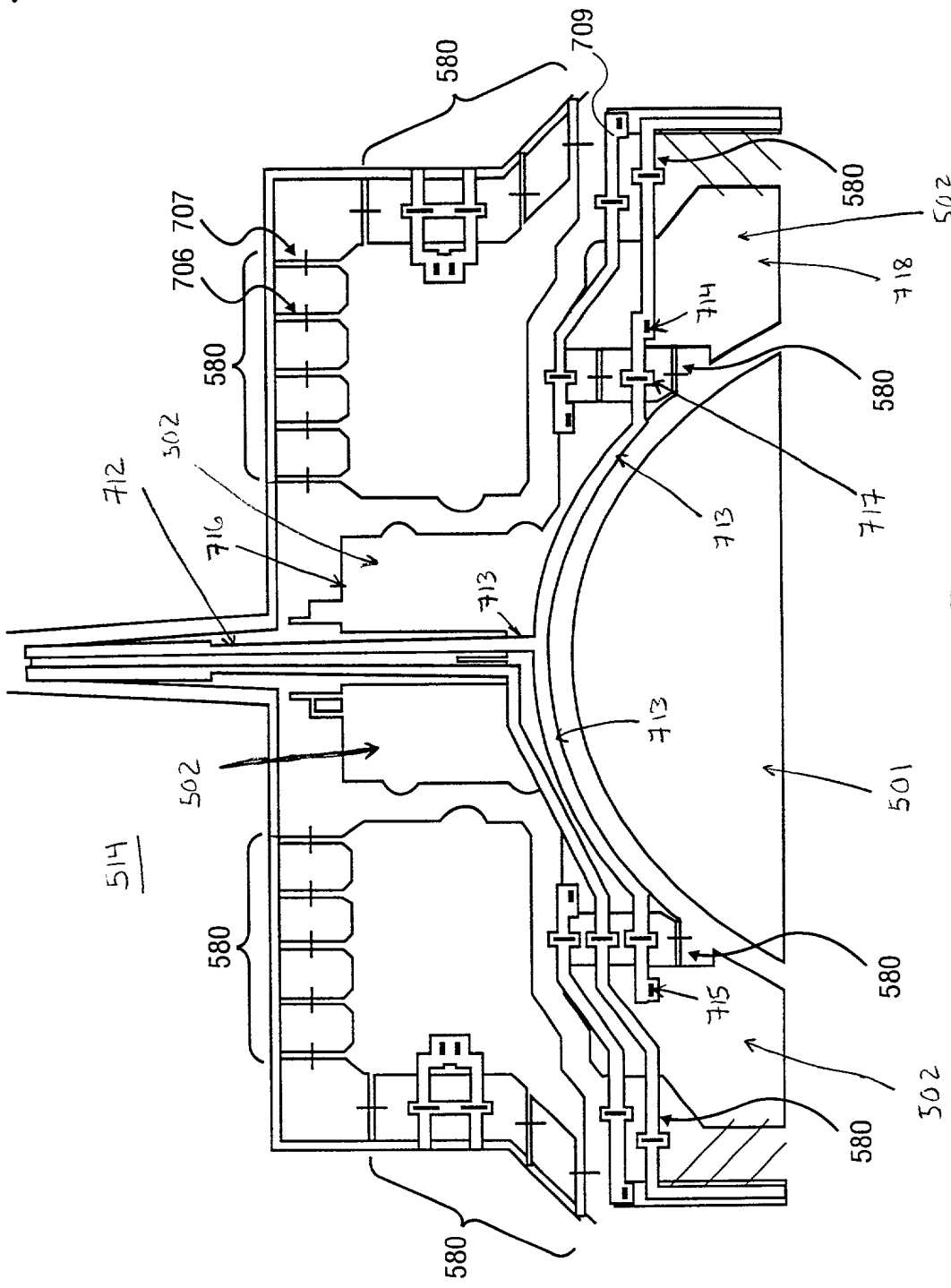


FIG. 7B

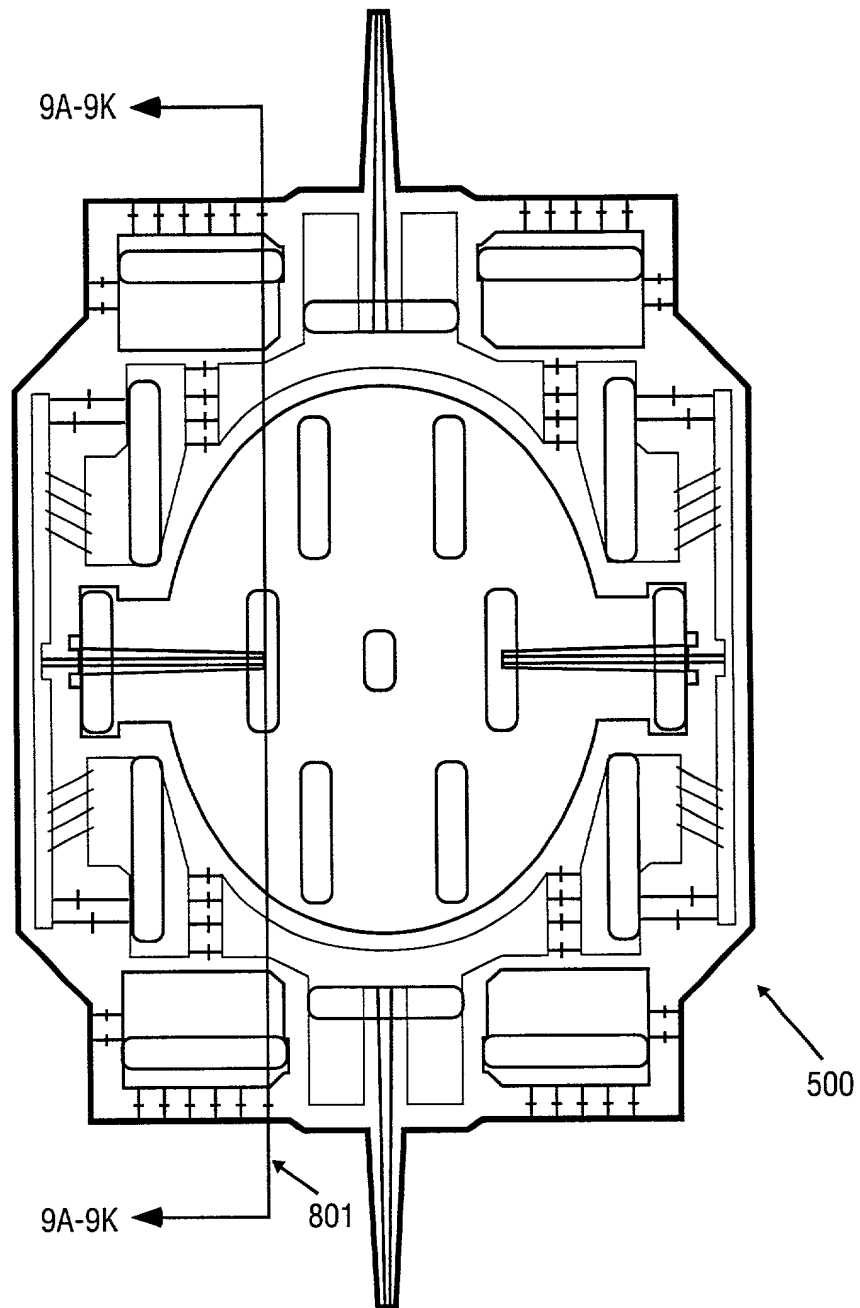


FIG. 8

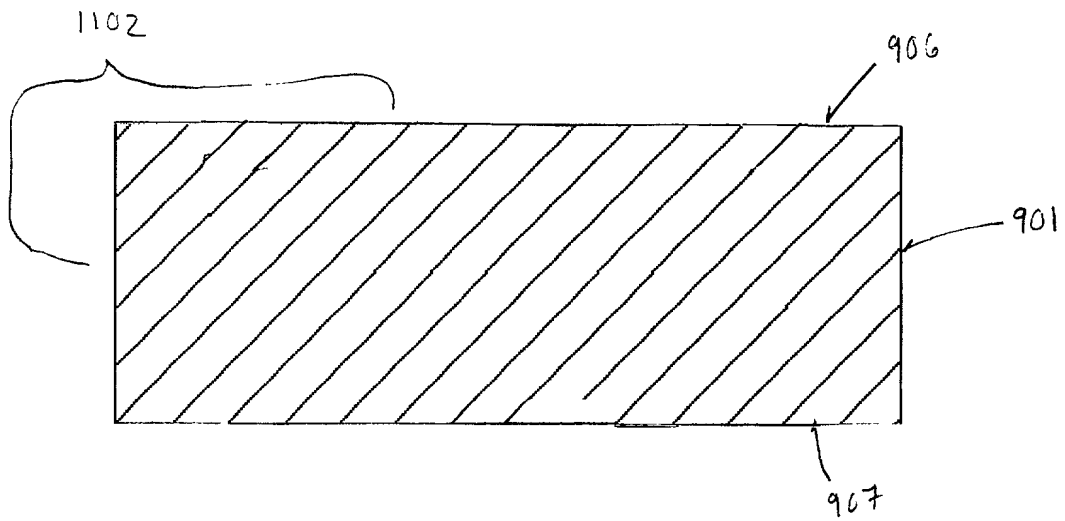


FIG. 9 A

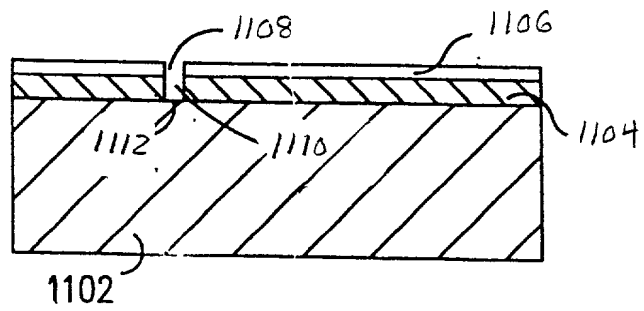


FIG. 9B

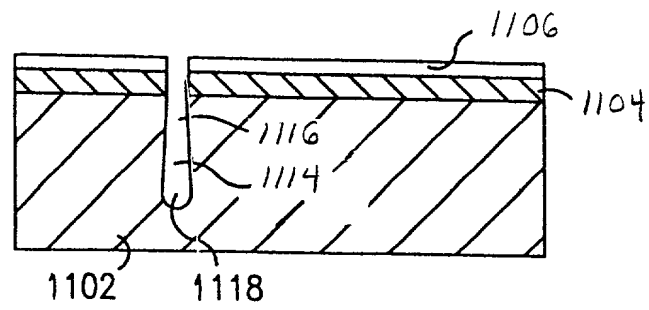


FIG. 9C

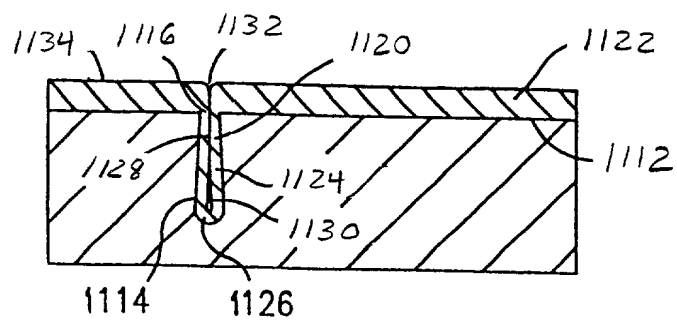


FIG. 9D

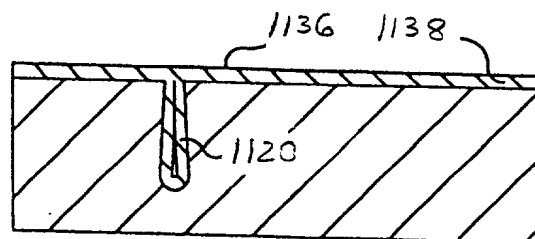
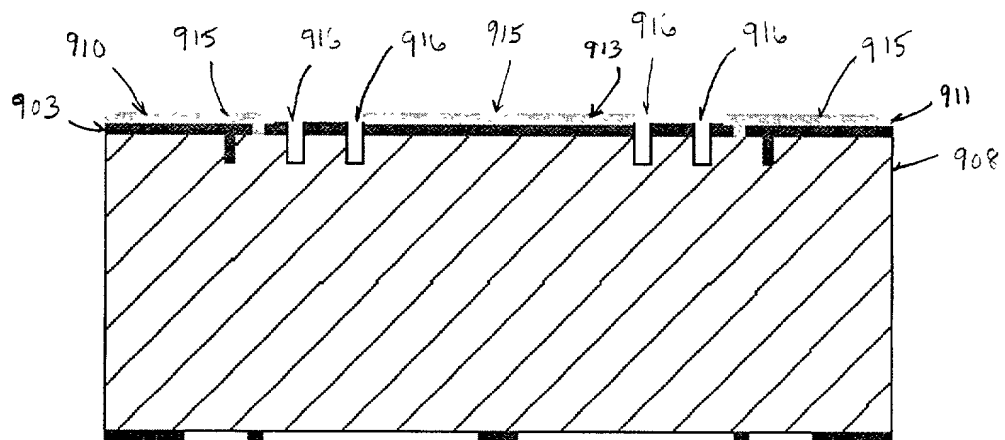
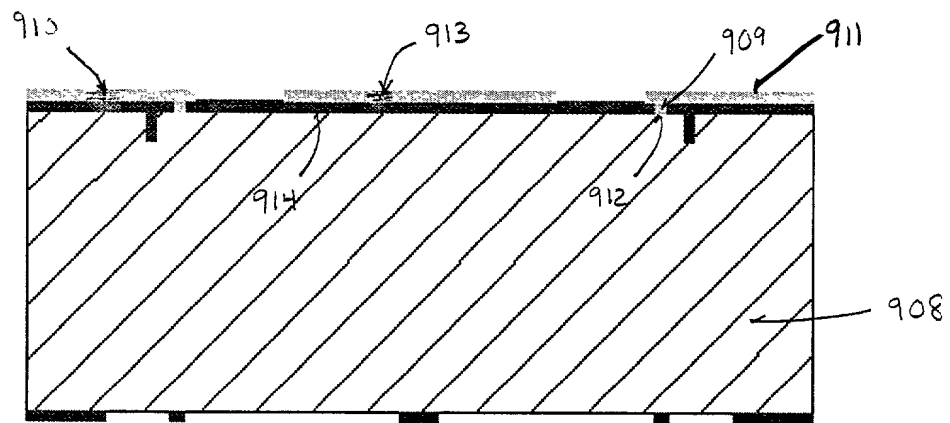
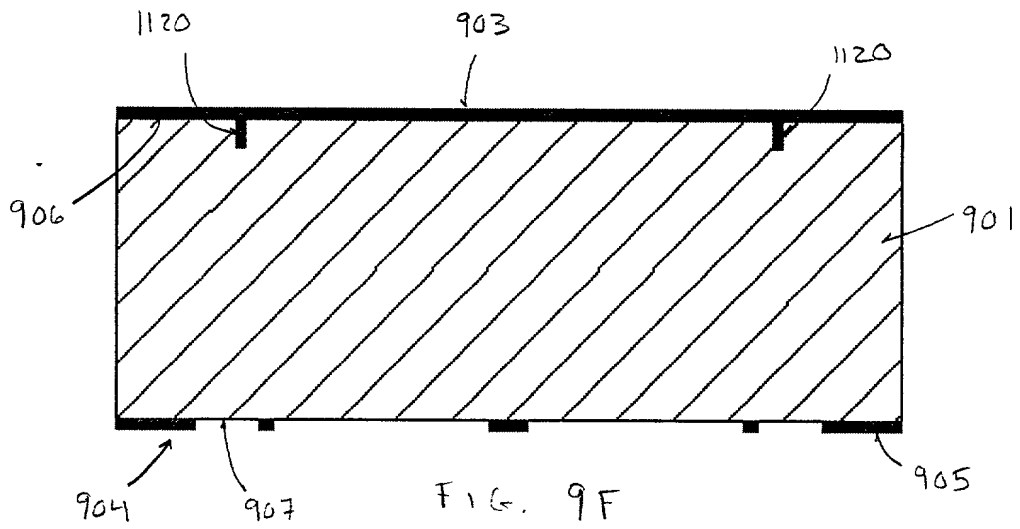
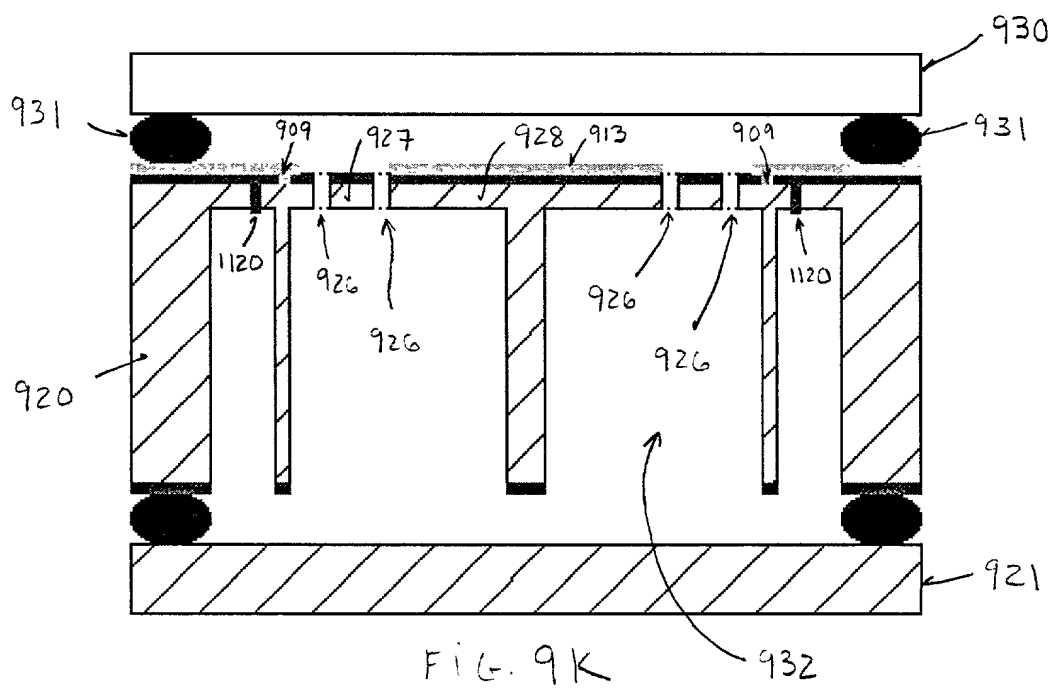
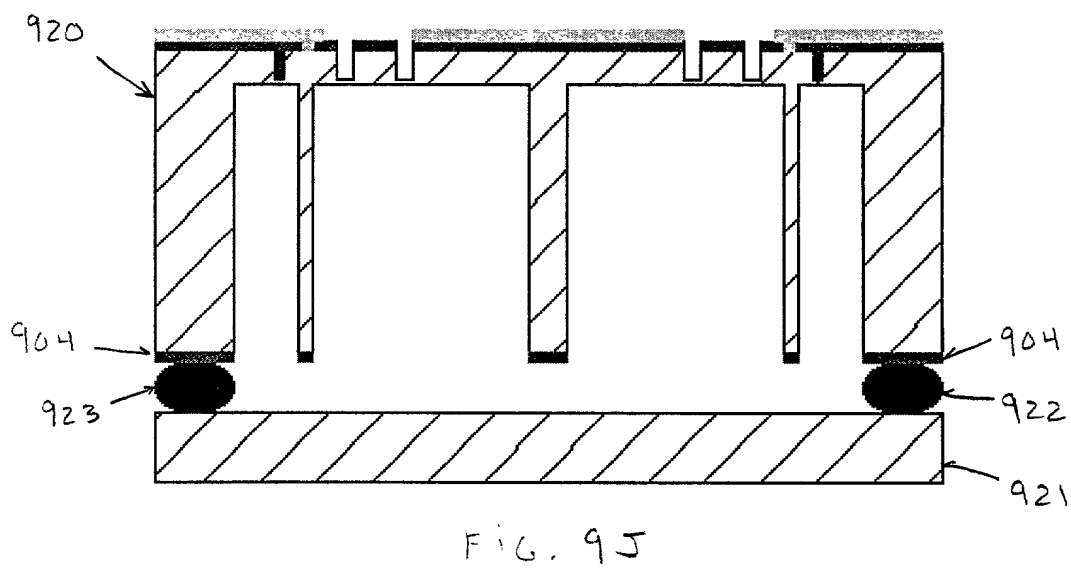
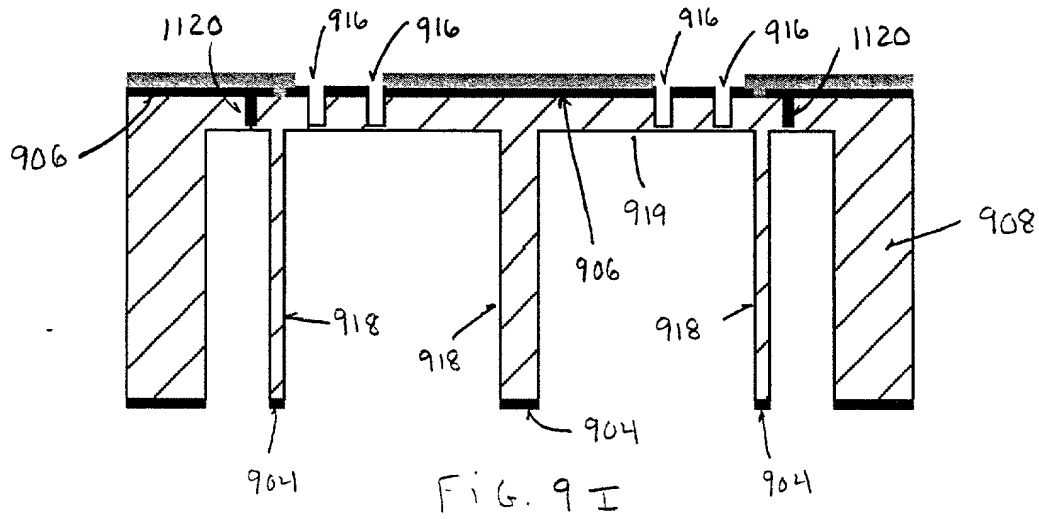
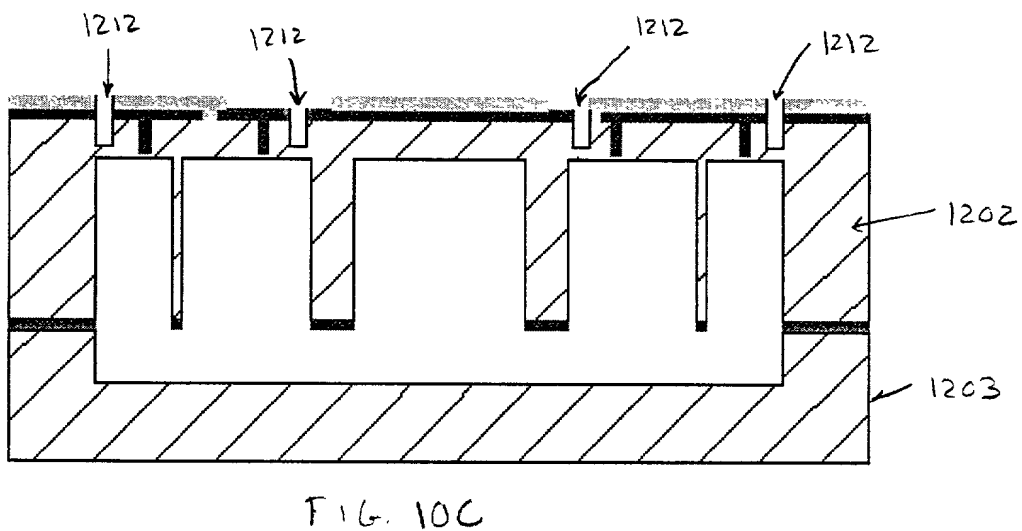
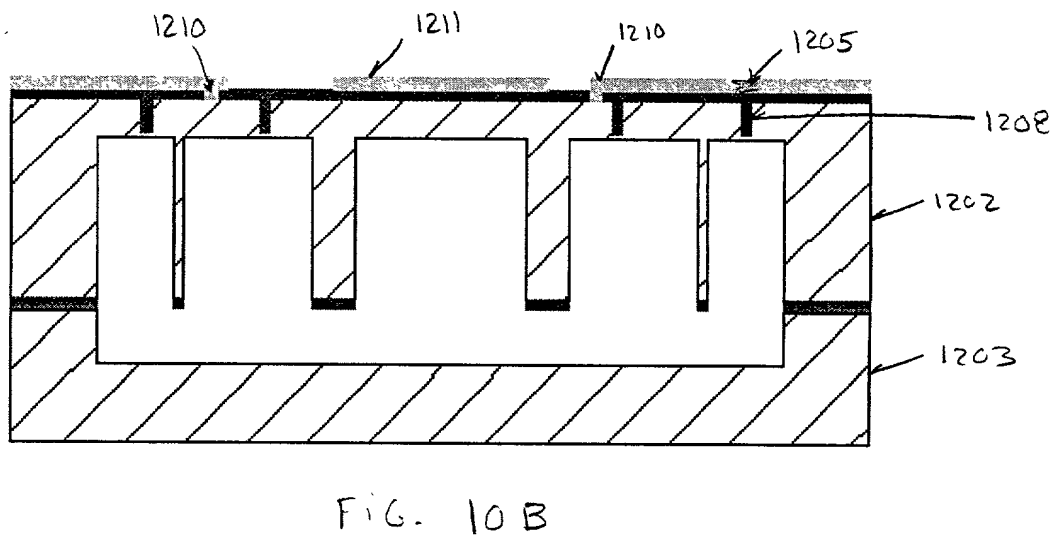
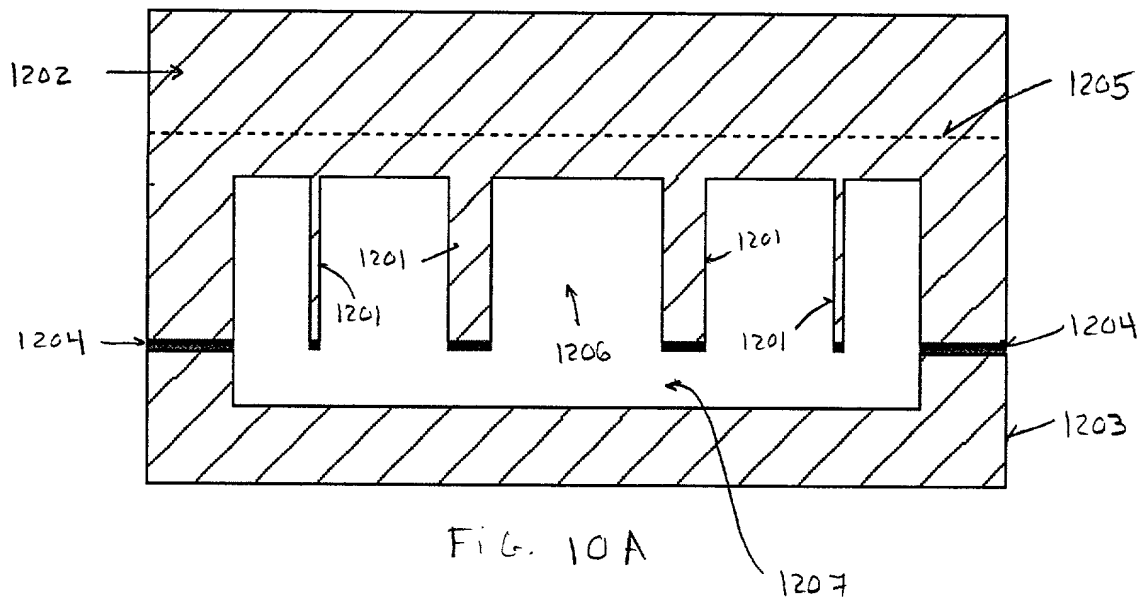
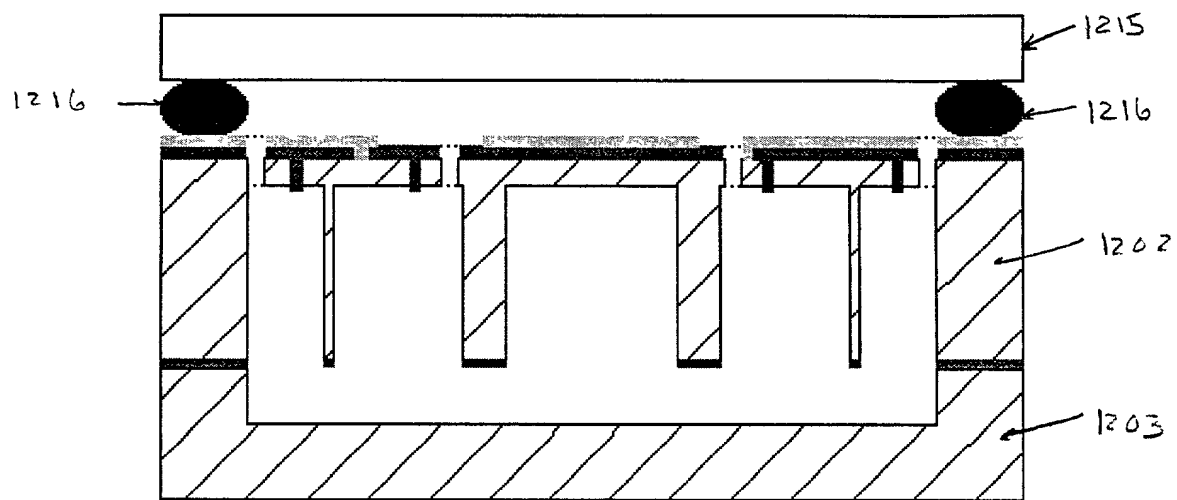
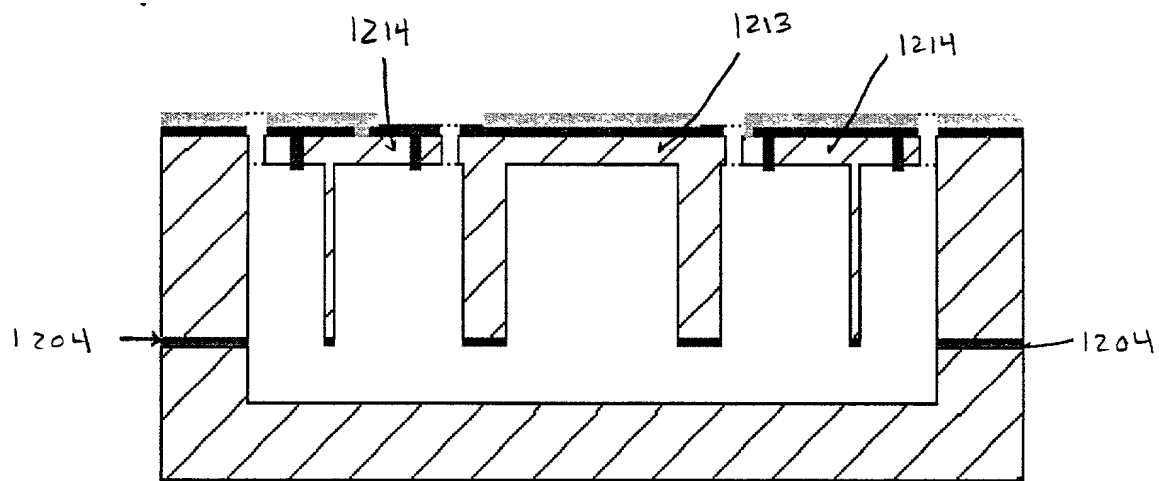


FIG. 9E









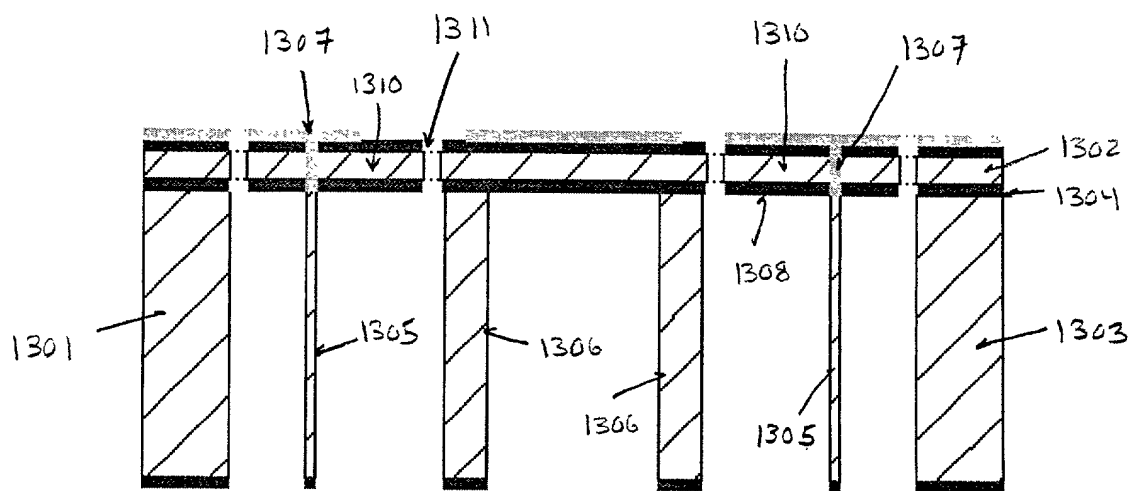
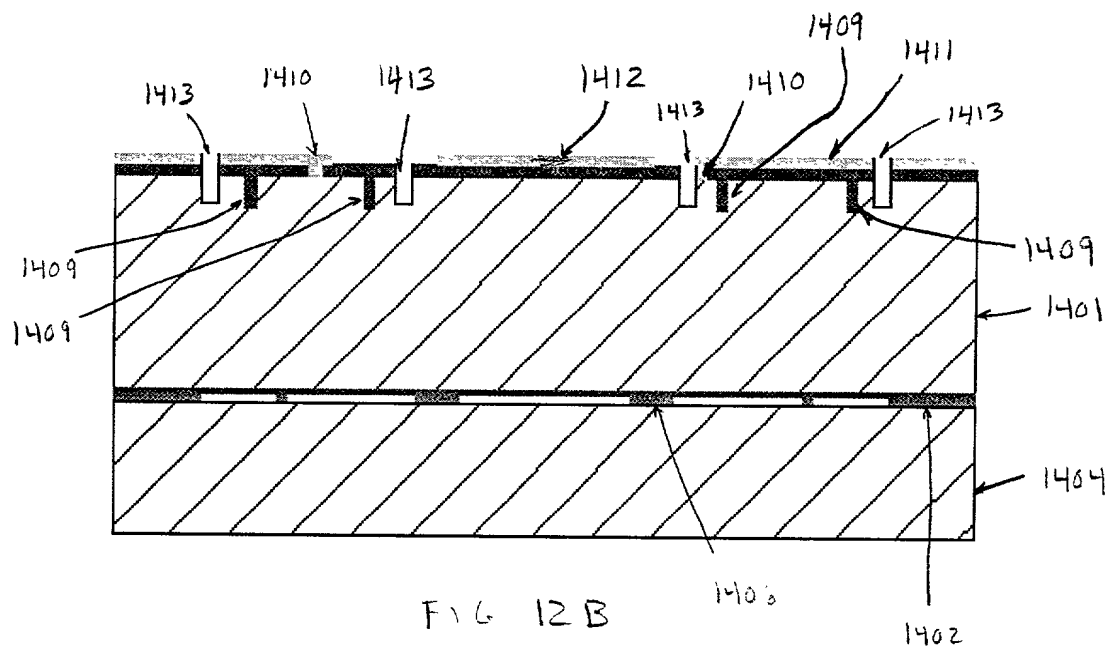
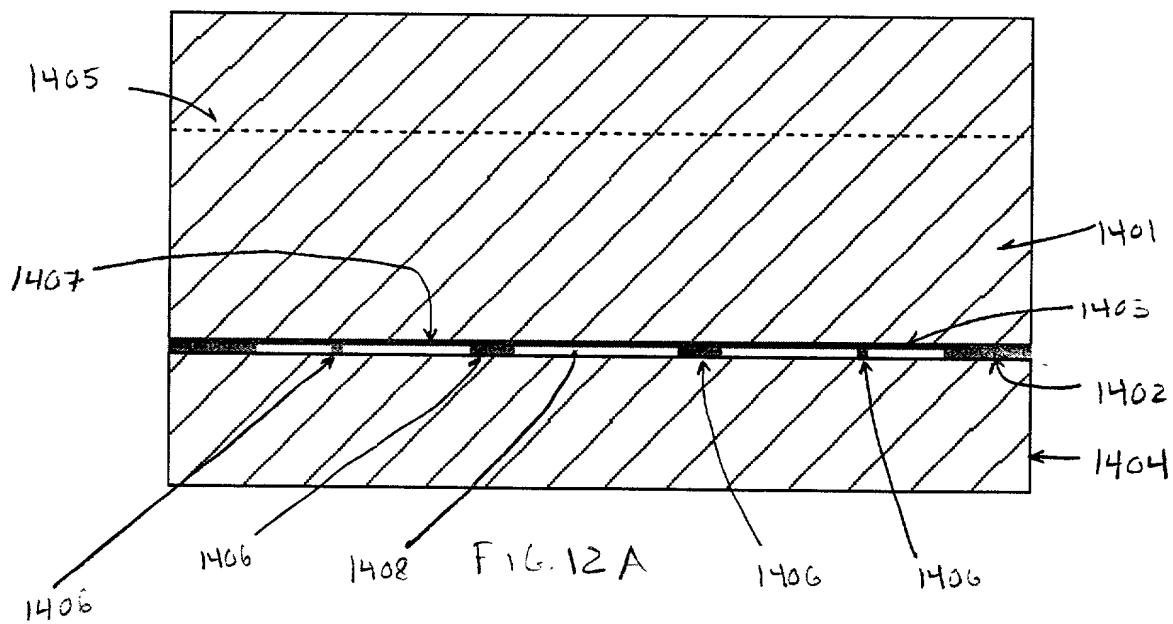


FIG. 11



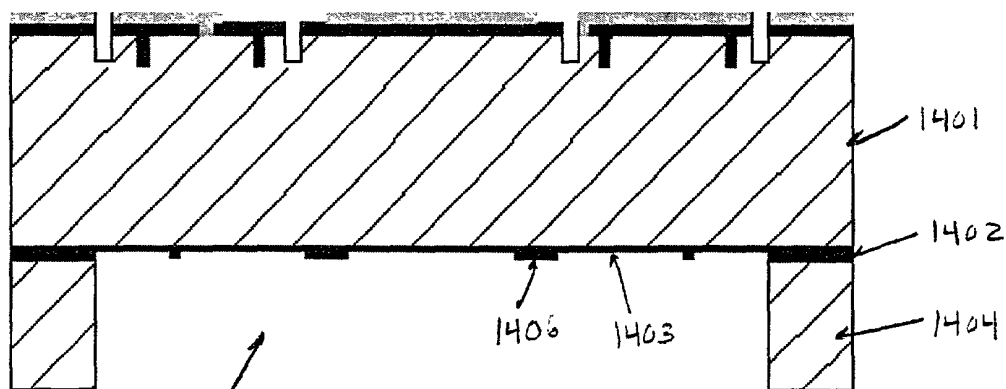


FIG. 12C

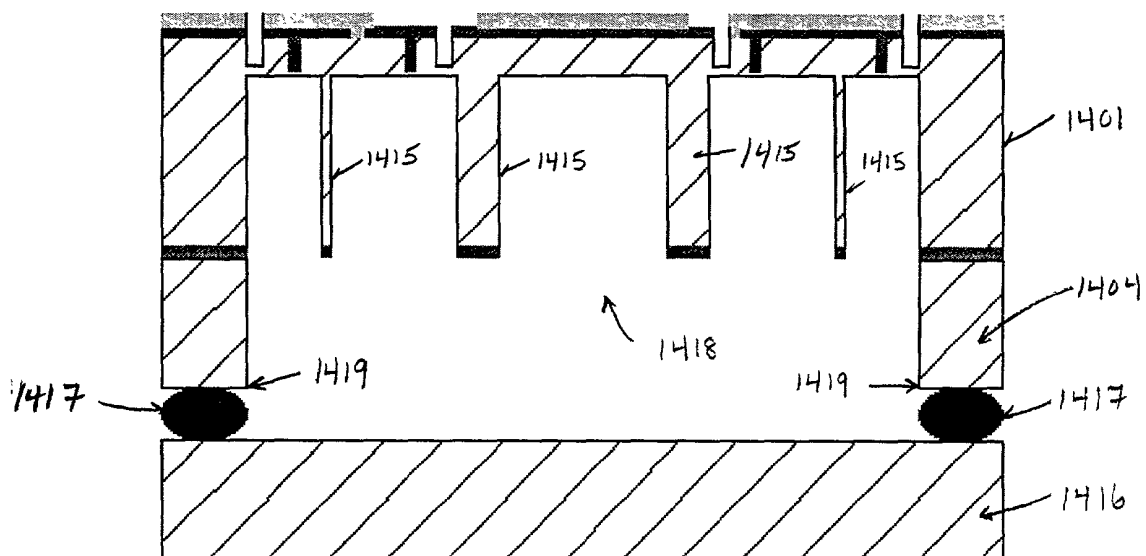


FIG. 12D

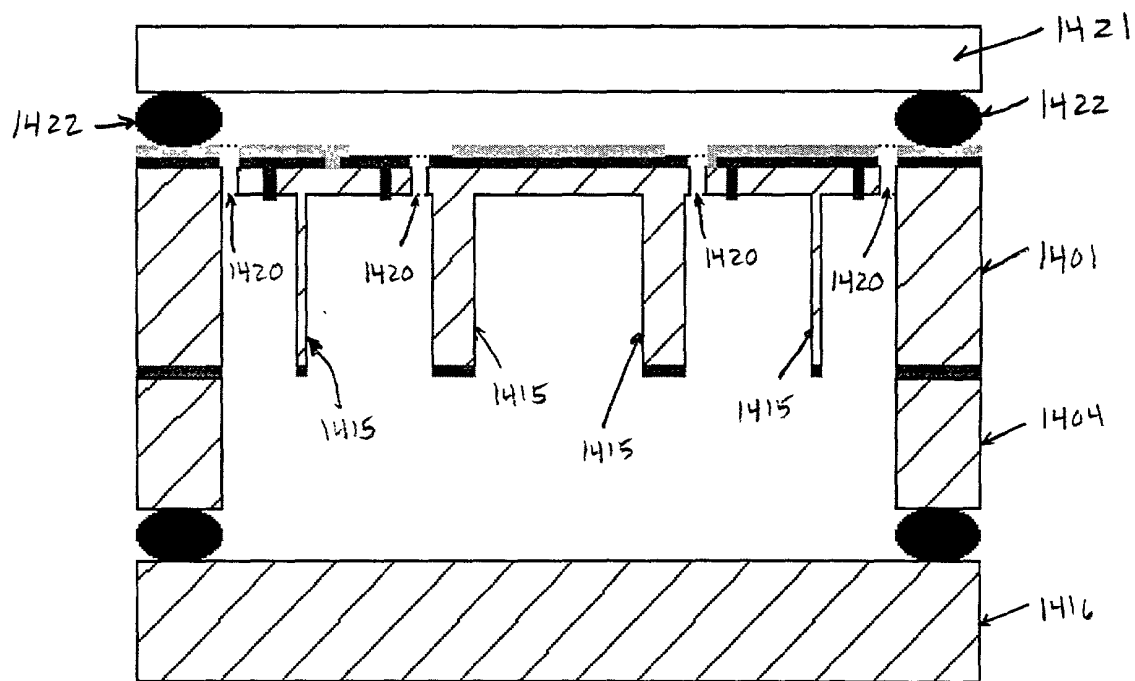


FIG 12E

FIG. 13A

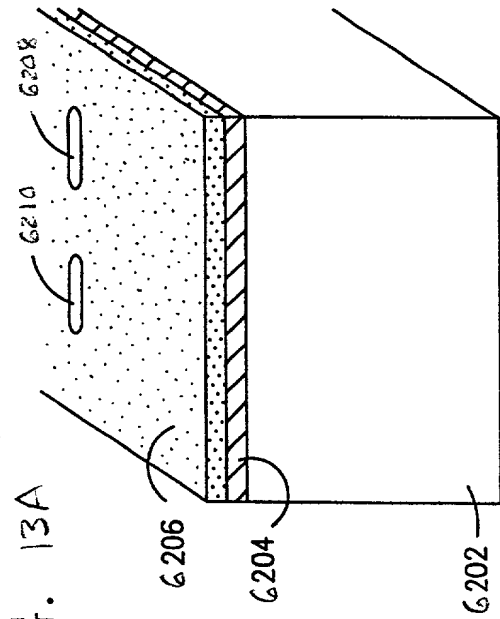


FIG. 13C

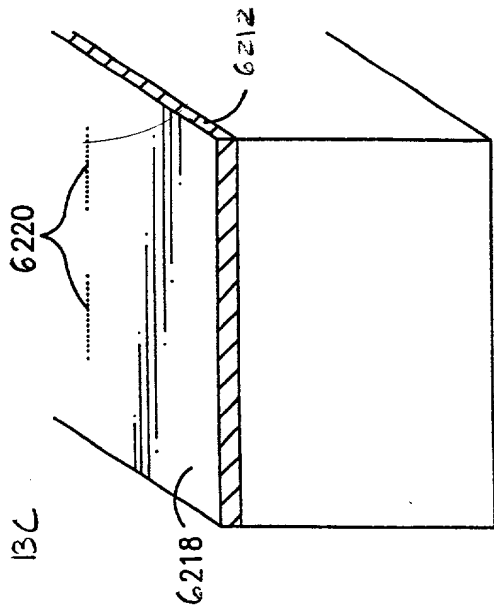


FIG. 13B

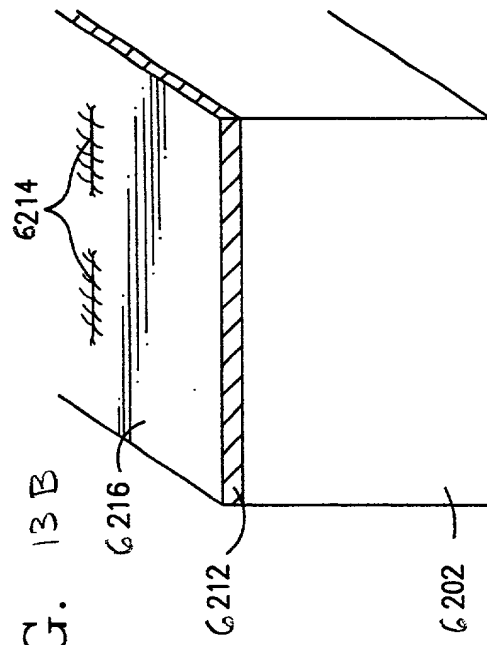
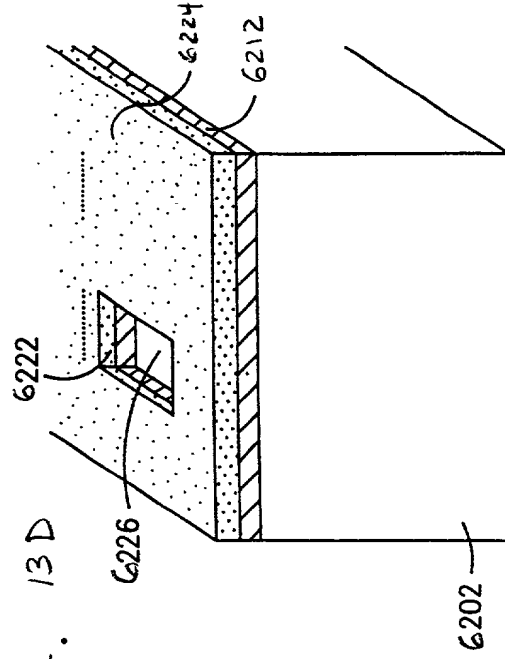


FIG. 13D



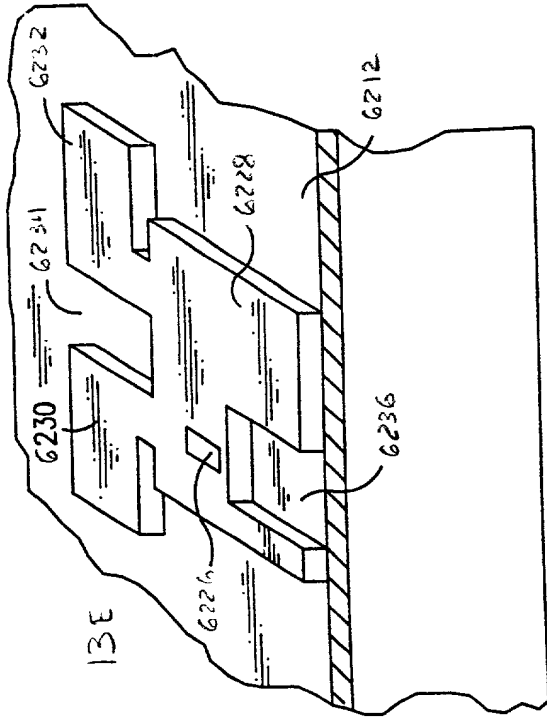


FIG. 13E

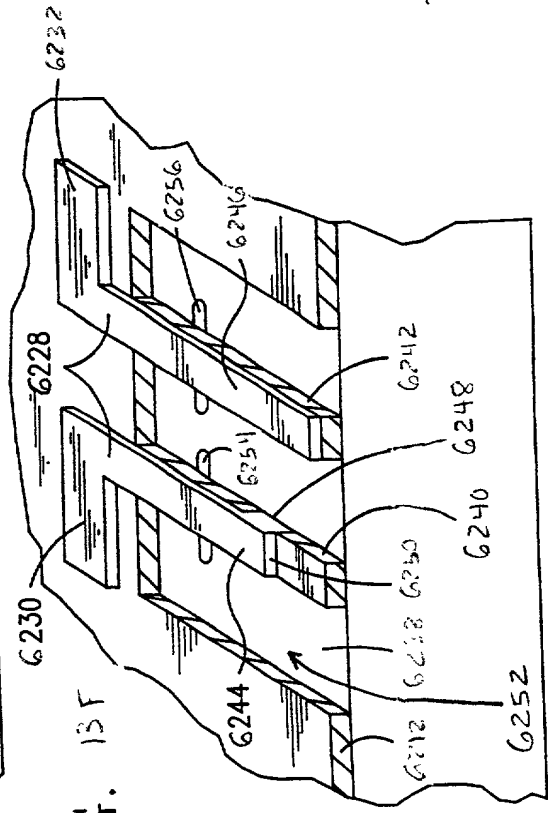


FIG. 13F

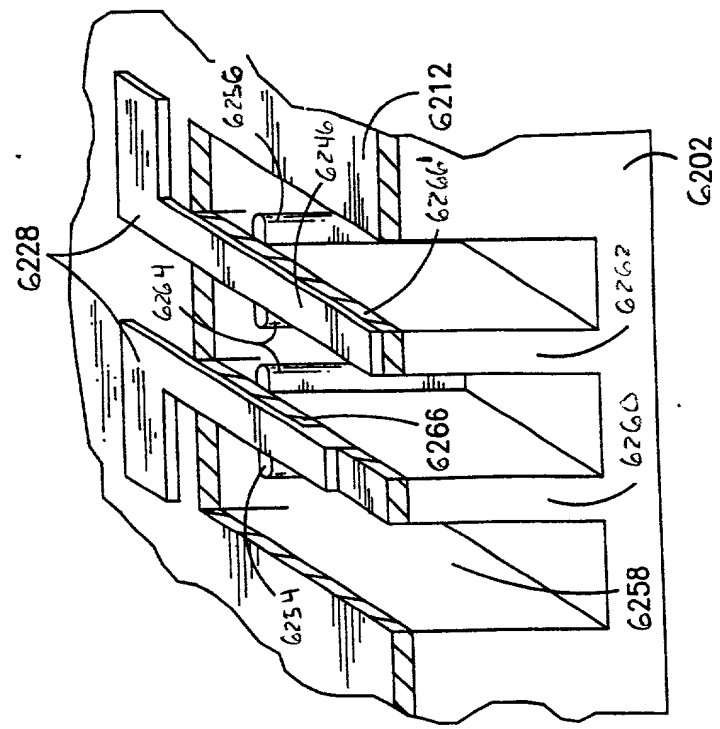


FIG. 13G

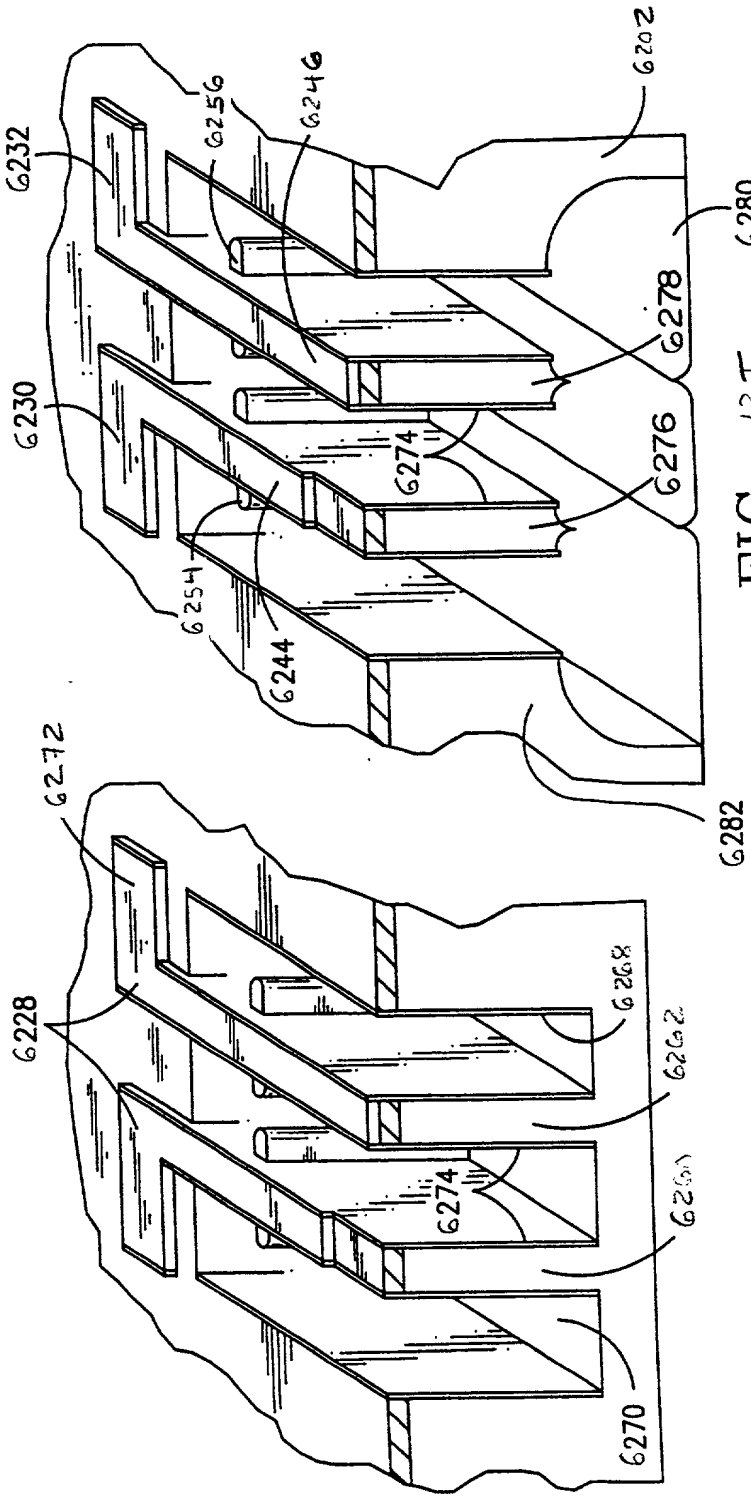


FIG. 13H

FIG. 13I